CH132 Datasheet

V1.3

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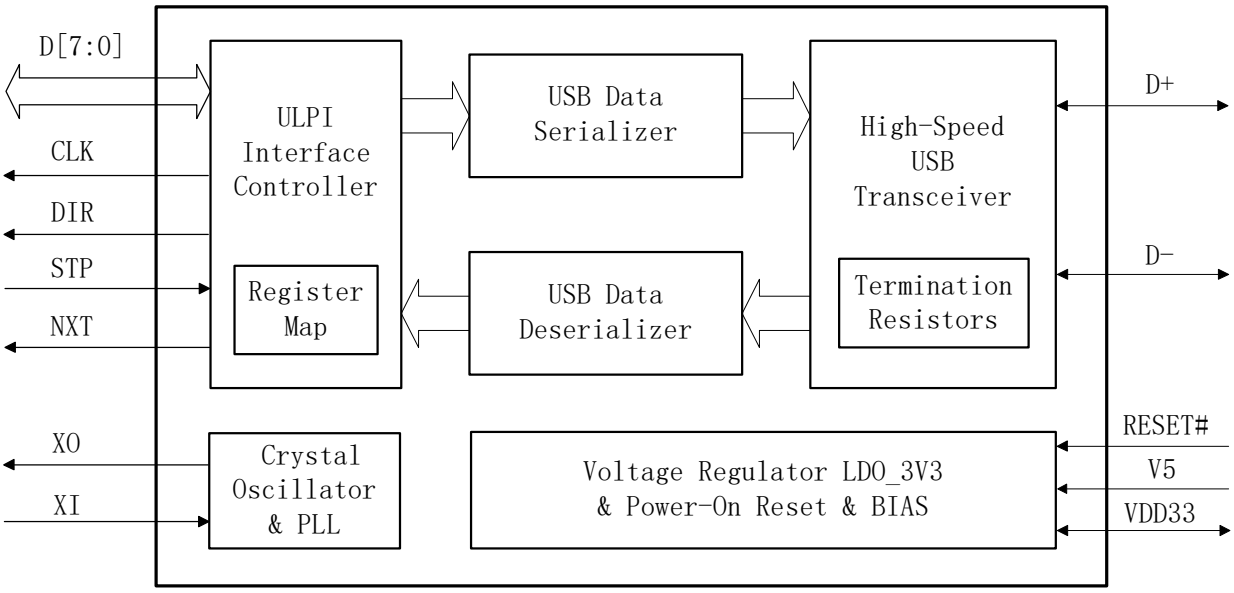
Overview

CH132 is a high-speed USB transceiver chip (USB PHY, High Speed Transceiver) with ULPI interface, compatible with USB 2.0 protocol specification and UTMI+ Low Pin Interface (ULPI) 1.1 protocol specification. It supports USB2.0 high-speed 480Mbps, full-speed 12Mbps and low-speed 1.5Mbps data transmission and reception, and can be used to extend the USB host port or device port for MCU or FPGA with ULPI interface.



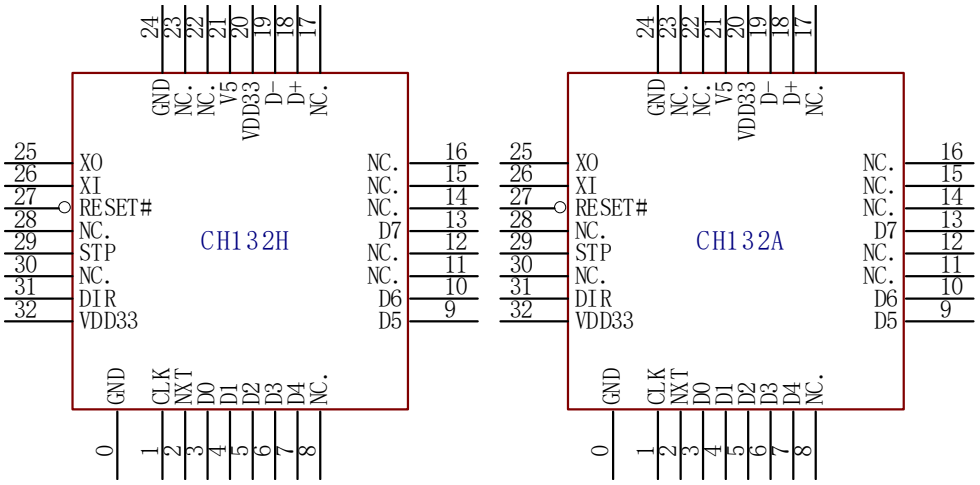
Features

- Compatible with USB Specification Rev. 2.0.
- Compatible with UTMI+ Low Pin Interface (ULPI) Rev 1.1.
- 12-pin ULPI interface, 3.3V I/O level, 60MHz clock.
- Support USB host and USB device.
- Support USB High-speed, Full-speed and Low-speed.
- Support 3-pin or 6-pin Full-Speed or Low-Speed serial mode.
- Built-in 3.3V low dropout linear regulator, support 3.3V to 5V supply input.
- Built-in power-on reset circuit, built-in clock oscillator and PLL.
- Built-in impedance matching resistor, built-in oscillation capacitor, with lower BOM cost.
- 6KV enhanced ESD performance.
- Industrial-grade temperature range: -40 to 85°C.
- Packages: QFN20, QFN32 and the others.

Chapter 1 Pin information

1.1 Pinouts

Figure 1-1 CH132H and CH132A pinouts



Note: Pin 0# is the EPAD of QFN package.

1.2 Packages

Table 1-1 Package description

Package form	Shaping width		Pin spacing		Package description	Order model
QFN32_5*5	5.0mm		0.5mm	19.7mil	Quad Flat No-lead Package	CH132H
QFN32_5*5	5.0mm		0.5mm	19.7mil	Quad Flat No-lead Package	CH132A

Note: CH132A is forward compatible with CH132H pin, some registers have different default values after reset.

1.3 Pin definitions

Table 1-2 CH132 pin definitions

Pin No.		Pin name	Type	Function Description
CH132H	CH132A			
18	18	D+	USB	USB2.0 high-speed differential signal lines DP
19	19	D-	USB	USB2.0 high-speed differential signal lines DM
1	1	CLK	O	ULPI 60 MHz clock signal output
2	2	NXT	O	ULPI Next signal output
31	31	DIR	O	ULPI Direction signal output
29	29	STP	I	ULPI Stop signal input, built-in controlled pull-up current
3	3	D0	I/O	ULPI bidirectional DATA0, built-in weak pull-down resistor

4	4	D1	I/O	ULPI bidirectional DATA1, built-in weak pull-down resistor
5	5	D2	I/O	ULPI bidirectional DATA2, built-in weak pull-down resistor
6	6	D3	I/O	ULPI bidirectional DATA3, built-in weak pull-down resistor
7	7	D4	I/O	ULPI bidirectional DATA4, built-in weak pull-down resistor
9	9	D5	I/O	ULPI bidirectional DATA5, built-in weak pull-down resistor
10	10	D6	I/O	ULPI bidirectional DATA6, built-in weak pull-down resistor
13	13	D7	I/O	ULPI bidirectional DATA7, built-in weak pull-down resistor
26	26	XI	I	Crystal input, external 12MHz crystal end, or external clock input
25	25	XO	O	Inverted output of crystal oscillator, need to connect the other end of the external 12MHz crystal
27	27	RESET#	I	Reset signal input, active low, built-in pull-up resistor
21	21	V5	P	5V or 3.3V power input, external 1uF~4.7uF decoupling capacitor
20	20	VDD33	P	LDO output and 3.3V power input, external 1uF~4.7uF decoupling capacitor
32	32	VDD33	P	3.3V power input, optional, but VDD33 connection recommended
24	24	GND	P	Common ground, optional but GND connection recommended
0	0	GND	P	Common ground (QFN EPAD), necessary connection
8, 11, 12, 14, 15, 16, 17, 22, 23, 28, 30	8, 11, 12, 14, 15, 16, 17, 22, 23, 28, 30	NC.	-	Empty or reserved pins, connection prohibited

Pin type:

(1) I: 3.3V signal input
(2) O: 3.3V signal output
(3) P: Power or ground
(4) USB: USB signal

Chapter 2 Basic functions

2.1 Clock and reset

2.1.1 Clock source

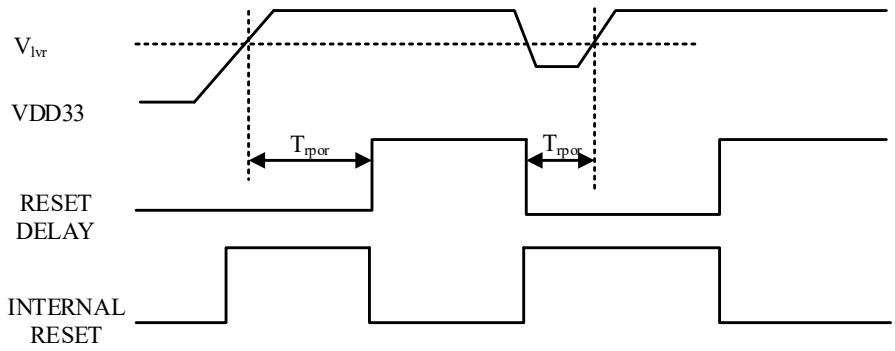
The CH132 requires a 12 MHz clock source, either by inputting the clock from pin XI and leaving XO suspended, or by connecting an external 12MHz crystal to pins XI and XO to generate the clock source via an internal oscillator. The CH132 then generates the multiple clocks required by the chip via PLL:

- 1.5MHz clock for USB low-speed data transfer
- 12MHz clock for USB full-speed data transfer
- 480MHz clock for USB high-speed data transfer
- 60MHz clock for ULPI controller
- Other clocks required for internal data processing

2.1.2 Power-on reset

The CH132 has a built-in power-on reset module, which generally does not require an external reset signal. When the power supply is powered on, the chip's internal POR power-on reset module will generate a power-on reset timing and delay Trpor to wait for the power supply to stabilize. During operation, when the power supply voltage falls below V_{lvr}, the chip's internal low voltage reset (LVR) module generates a low voltage reset until the voltage rises back up and delays for the power supply to stabilize. Figure 2-1 shows the power-on reset process as well as the low voltage reset process.

Figure 2-1 Power-on reset



2.1.3 External reset

The external reset input pin RESET# contains a pull-up resistor of about 24KΩ, and if the chip needs to be reset externally, the pin can be driven low (open-drain drive is recommended) with a low pulse width of at least Twreset. It is recommended not to attach an external pull-up resistor.

2.2 Power supply

The CH132 has a built-in low dropout linear regulator LDO. 3.3V supply by default, 5V supply is also supported. For 3.3V powered systems, the 3.3V supply is fed to both VDD33 pin and V5 pin for internal analogue and I/O circuits. For 5V supply systems, the 5V supply is input to V5 pin and the internal LDO generates a 3.3V supply at VDD33 pin for internal analogue and I/O circuits. In both cases, the VDD33 pin and the V5 pin require external decoupling capacitors. When 5V power supply is selected, the CH132H support voltage range is 3.7V~4.5V for the number of the 4th digit in the special lot number, and the CH132H support voltage range for CH132A or other lot numbers is 4.5V~5.25V.

Avoid feeding the 5V power from VBUS directly into V5 pin. It is recommended that an overvoltage protection circuit be added between VBUS pin and V5 pin.

2.3 USB transceiver

The CH132 USB transceiver takes on USB high-speed, full-speed and low-speed data transceiver tasks. Transceiver includes the differential driver circuitry necessary for USB high-speed, full-speed and low-speed data transmission, the differential and single ended receivers for USB high-speed, full-speed and low-speed data reception, the circuitry to detect high-speed bus activity and the circuitry to detect high-speed bus disconnection. The USB port has a variety of built-in matching resistors, including impedance matching resistors, device pull-up resistors, host pull-down resistors, etc.

A detailed relationship between the registers and the USB port mode can be found in Table 2-1 below.

Table 2-1 Register settings and port mode relationships

USB port mode	Register settings				
	XCVR SELECT[1:0]	TERM SELECT	OP MODE[1:0]	DP_ PULLDOWN	DM_ PULLDOWN
3-state drivers	xxb	xb	01b	xb	xb
Host Chirp	00b	0b	10b	1b	1b
Host High-speed	00b	0b	00b	1b	1b
Host Full-speed	x1b	1b	00b	1b	1b
Host High-speed or Full-speed suspend	01b	1b	00b	1b	1b
Host High-speed or Full-speed resume	01b	1b	10b	1b	1b
Host Low-speed	10b	1b	00b	1b	1b
Host Low-speed suspend	10b	1b	00b	1b	1b
Host Low-speed resume	10b	1b	10b	1b	1b
Host Test J or Test K	00b	0b	10b	1b	1b
Peripheral Chirp	00b	1b	10b	0b	0b
Peripheral High-speed	00b	0b	00b	0b	0b
Peripheral Full-speed	01b	1b	00b	0b	0b
Peripheral High-speed or Full-speed suspend	01b	1b	00b	0b	0b
Peripheral High-speed or Full-speed resume	01b	1b	10b	0b	0b
Peripheral Test J or Test K	00b	0b	10b	0b	0b

2.4 ULPI controller

The CH132 provides a 12 Pin interface compatible with the ULPI (UTMI+ Low Pin Interface) 1.1 protocol. This interface should be connected to the ULPI interface of the ULPI LINK, which has a USB controller at the other end.

This ULPI interface controller has the following functions:

- ULPI protocol compatible interface and register settings
- Allow functional control via USB host or peripheral devices
- Parse data transmitted or received by USB
- Prioritize USB data transmitting and receiving, interrupts and register operations
- 3-pin serial mode
- 6-pin serial mode

2.5 ULPI RX CMD data

Table 2-2 RXCMD data bit format

<table>
<tr><th>Bit</th><th>Name</th><th>Default</th><th colspan="4">Description</th></tr>
<tr><td>[1:0]</td><td>LineState</td><td>00b</td><td colspan="4">Corresponds to UTMI+ LineState two signals:
LineState[0] corresponds to receiving single-ended data from DP,
LineState[1] corresponds to receiving single-ended data from DM.</td></tr>
<tr><td>[3:2]</td><td>Reserved</td><td>00b</td><td colspan="4">Reserved, always 00.</td></tr>
<tr><td rowspan="6">[5:4]</td><td rowspan="6">RxEvent</td><td rowspan="6">00b</td><td colspan="4">UTMI event signal encoding:</td></tr>
<tr><td>Value</td><td>RxActive</td><td>RxError</td><td>HostDisconnect</td></tr>
<tr><td>00</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>01</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>11</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>10</td><td>X</td><td>X</td><td>1</td></tr>
<tr><td>6</td><td>Reserved</td><td>0b</td><td colspan="4">Reserved, always 0.</td></tr>
<tr><td>7</td><td>Reserved</td><td>0b</td><td colspan="4">Reserved, data should be ignored.</td></tr>
</table>

2.6 3-pin and 6-pin serial mode

The CH132 provides either 3-pin or 6-pin serial modes. Select the serial mode of the 3-wire or 6-wire interface as needed to transfer full-speed or low-speed USB packets. 3-wire serial mode interface mapping is shown in Table 2-3, and 6-wire serial mode interface mapping is shown in Table 2-4.

Entering or exiting the 3-pin or 6-pin serial mode can be described in the R8_INTF_CTRL register regarding the 3PIN_FSLS_SERIAL or 6PIN_FSLS _SERIAL bit is described.

Table 2-3 Signal mapping for 3-pin serial

Signal	Maps to	Direction	Description
TX_ENABLE	DATA0	I	Mode selection, transmit enable. Active high. 0: Receive data; 1: Transmit data.
DAT	DATA1	I/O	When TX_ENABLE = 1, transmit differential data on DP and DM. When TX_ENABLE = 0, receive differential data from DP and DM.
SE0	DATA2	I/O	When TX_ENABLE = 1, transmit single-ended zero on DP and DM. When TX_ENABLE = 0, receive single-ended zero from DP and DM.
Reserved	DATA3	O, PD	Reserved, CH132 pin output data should be ignored.
Reserved[7:4]	DATA[7:4]	O, PD	Reserved, CH132 pin provides pull-down resistor or output low.

Table 2-4 Signal mapping for 6-pin serial

Signal	Maps to	Direction	Description
TX_ENABLE	DATA0	I	Transmit enable. Active high.

TX_DAT	DATA1	I	Transmit differential data on DP and DM
TX_SE0	DATA2	I	Transmit single-ended zero on DP and DM
Reserved	DATA3	O, PD	Reserved, CH132 pin output data should be ignored.
RX_DP	DATA4	O	Receive single-ended data from DP
RX_DM	DATA5	O	Receive single-ended data from DM
RX_RCV	DATA6	O	Receive differential data from DP and DM
Reserved	DATA7	O, PD	Reserved, CH132 pin provides pull-down resistor or output low.

Chapter 3 ULPI registers

3.1 Register description

The following abbreviations may be used in this datasheet when describing registers:

Register bit attributes	Description
RO	Read-only. Data is generated and changed by hardware.
WO	Write-only (This bit cannot be read, and the read value is uncertain)
RW	Readable and writable.

CH132 series chip ULPI interface operation-related register description, the default based on CH132A, other models if different plus note.

Table 3-1 CH132 ULPI registers

Name	Address (6 bit)				Description	Reset Value
	Read	Write	Set	Clear		
ID	0x00–0x03				ID register. Reserved	0x00000000
R8_FUNC_CTRL	0x04–0x06	0x04	0x05	0x06	ULPI function control register	0x41 [Note 1]
R8_INTF_CTRL	0x07–0x09	0x07	0x08	0x09	ULPI interface control register	0x00
R8_OTG_CTRL	0x0A–0x0C	0x0A	0x0B	0x0C	OTG control register	0x06 [Note 2]
R8_USB_INTR_EN_R	0x0D–0x0F	0x0D	0x0E	0x0F	USB rising interrupt enable register	0x01 [Note 2]
R8_USB_INTR_EN_F	0x10–0x12	0x10	0x11	0x12	USB falling interrupt enable register	0x01 [Note 2]
R8_USB_INTR_STAT	0x13	-	-	-	USB interrupt status register	0x00
R8_USB_INTR_L	0x14	-	-	-	USB interrupt latch register	0x00
R8_SCRATCH	0x16–0x18	0x16	0x17	0x18	Scratch register	0x00
	Other				Reserved	0x00

(1) R: Read, readable register. Read-only if there is no corresponding W/S/C.

(2) W: Write, the register is written, the new data will overwrite the original data of this register directly during the operation.

(3) S: Set, register by position 1, the new data will be written with the original data of this register by bit or operation.

(4) C: Clear, the register is cleared by bit, the new data will be written with the original data of this register after bit and operation.

Note 1: Default is based on CH132A (same below), for CH132H it is 0x4D.

Note 2: 0x00 for CH132H.

Recommendation:

Set the target parameters to the R8_FUNC_CTRL and R8_OTG_CTRL registers after each power-up or reset, regardless of the original values.

No need to manipulate and use each register of R8_USB_INTR_*, which can be implemented with RxEvent/LineState status in RXCMD.

ULPI function control register (R8_FUNC_CTRL, Address R = 04h/05h/06h, W = 04h, S = 05h, C = 06h)

Bit	Symbol	Access	Description	Reset Value
7	Reserved	RW	Reserved	0b

6	SUSPEND	RW	**Suspend:** Enter low-power mode. Active low. The ULPI linker can exit low power mode through STP. This bit is automatically set to 1 when the CH132 exits low power mode. **0**: Low power mode. **1**: Normal. *Note: CH132H does not support low-power consumption.*	1b
5	RESET	RW	**Internal Reset:** Active high. This does not reset the ULPI interface or the ULPI register. When the reset is completed, the CH132 will desert DIR and automatically clear this bit. **0**: Normal; **1**: Enable reset. *Note: CH132H disables this bit.*	0b
[4:3]	OP MODE	RW	**Operation Mode:** Selects the required bit-encoding style during transfer **00**: Normal; **01**: Not drive; **10**: Disable bit-stuffing and NRZI encoding; **11**: Reserved.	00b [Note 3]
2	TERM SELECT	RW	**Termination selection:** Controls the pull-up/pull-down resistor and high-speed terminations, depending on XCVR SELECT, OP MODE, DP_PULLDOWN and DM_PULLDOWN. As shown in Table 2-1	0b [Note 4]
[1:0]	XCVR SELECT	RW	**Transceiver selection:** **00**: Enable the high-speed transceiver **01**: Enable the full-speed transceiver **10**: Enable the low-speed transceiver **11**: Enable the full-speed transceiver for low-speed packets (full-speed preamble is automatically prefixed)	01b

Note 3:01b for CH132H.
Note 4:1b for CH132H.

ULPI interface control register (R8_INTF_CTRL, Address R = 07h/08h/09h, W = 07h, S = 08h, C = 09h)

Bit	Symbol	Access	Description	Reset Value
7	INTF_PROT_DIS	RW	**Disable interface protect:** The ULPI interface protection circuitry built into the control chip when the ULPI linker is not output to STP and DATA[7:0] **0**: Enable ULPI interface protection circuit, enable STP weak pull-ups; **1**: Disable ULPI interface protection circuit, disable STP weak pull-ups.	0b
[6:2]	Reserved	RW	Reserved	00000b
1	3PIN_FSLS_SERIAL	RW	**3-Pin full-speed and low-speed serial mode:** Changes the ULPI interface into a 3-pin serial interface. The CH132 automatically clears this bit when the mode is exited.	0b

			0: Disables 3-pin serial mode, full-speed low-speed packet transfer via ULPI parallel port; **1**: Enables 3-pin serial mode, full-speed low-speed packet transmission over 3-pin interface	
0	6PIN_FSLS_SERIAL	RW	**6-Pin full-speed and low-speed serial mode:** Changes the ULPI interface into a 3-pin serial interface. The CH132 will automatically clear this bit when the mode is exited. **0**: Disables 6-pin serial mode, full-speed low-speed packet transfer via ULPI parallel port; **1**: Enables 6-pin serial mode, full-speed low-speed packet transmission over 6-pin interface	0b

OTG control register (R8_OTG_CTRL, Address R = 0Ah/0Bh/0Ch, W = 0Ah, S = 0Bh, C = 0Ch)

Bit	Symbol	Access	Description	Reset Value
[7:3]	Reserved	RW	Reserved	00000b
2	DM_PULLDOWN	RW	**DM pull-down enable:** **0:** DM pull-down resistor disabled **1:** DM pull-down resistor enabled	1b [Note 5]
1	DP_PULLDOWN	RW	**DP pull-down enable:** **0:** DP pull-down resistor disabled **1:** DP pull-down resistor enabled	1b [Note 5]
0	Reserved	RW	Reserved	0b

Note 5:0b for CH132H.

USB rising interrupt enable register (R8_USB_INTR_EN_R, Address R = 0Dh/0Eh/0Fh, W = 0Dh, S = 0Eh, C = 0Fh)

Bit	Symbol	Access	Description	Reset Value
[7:1]	Reserved	RW	Reserved	0000000b
0	HOST_DISCON_R	RW	**Host disconnect rise:** Enable Interrupts for logic 0 to logic 1 transitions on HOST_DISCON	1b [Note 5]

USB falling interrupt enable register (R8_USB_INTR_EN_F, Address R = 10h/11h/12h, W = 10h, S = 11h, C = 12h)

Bit	Symbol	Access	Description	Reset Value
[7:1]	Reserved	RW	Reserved	0000000b
0	HOST_DISCON_F	RW	**Host disconnect rise:** Enable Interrupts for logic 1 to logic 0 transitions on HOST_DISCON	1b [Note 5]

USB interrupt status register (R8_USB_INTR_STAT, Address R = 13h)

Bit	Symbol	Access	Description	Reset Value
[7:1]	Reserved	RO	Reserved	0000000b
0	HOST_DISCON	RO	**Host disconnect:** Provides UTMI+ host port disconnect status values. **0**: Connected, USB device detected on host port; **1**: Disconnected, no USB device connection detected Only supports high-speed USB disconnect detection, not full-speed and low-speed disconnect detection.	0b

USB interrupt latch register (R8_USB_INTR_L, Address R = 14h)

Bit	Symbol	Access	Description	Reset Value
[7:1]	Reserved	RO	Reserved	0000000b
0	HOST_DISCON	RO	**Host disconnect latch:** Automatically set when an unmasked event occurs on HOST_DISCON. CLEARED when this register is READ	0b

SCARTCH register (R8_SCARTCH, Address R = 16h)

Bit	Symbol	Access	Description	Reset Value
[7:0]	SCARTCH	RW	Registers used for testing, readable and writable, without affecting chip functionality	00000000b

Chapter 4 Parameters

4.1 Absolute maximum ratings (Critical or exceeding the absolute maximum value may cause the chip to operate improperly or even be damaged.)

Symbol	Parameter description	Min.	Max.	Unit
TA	Operating ambient temperature	-40	85	℃
TS	Storage ambient temperature	-55	150	℃
V5	LDO input voltage (pin V5 to power, pin GND to ground)	-0.4	5.5	V
VDD33	3.3V source voltage (pin VDD33 to power, pin GND to ground)	-0.4	4.0	V
VUSB	Voltage on USB signal pins	-0.4	VDD33+0.4	V
VIO	Voltage on other input or output pins (excluding XI and XO)	-0.4	VDD33+0.4	V
VESD	HBM ESD withstand voltage on I/O pins	5K	7K	V

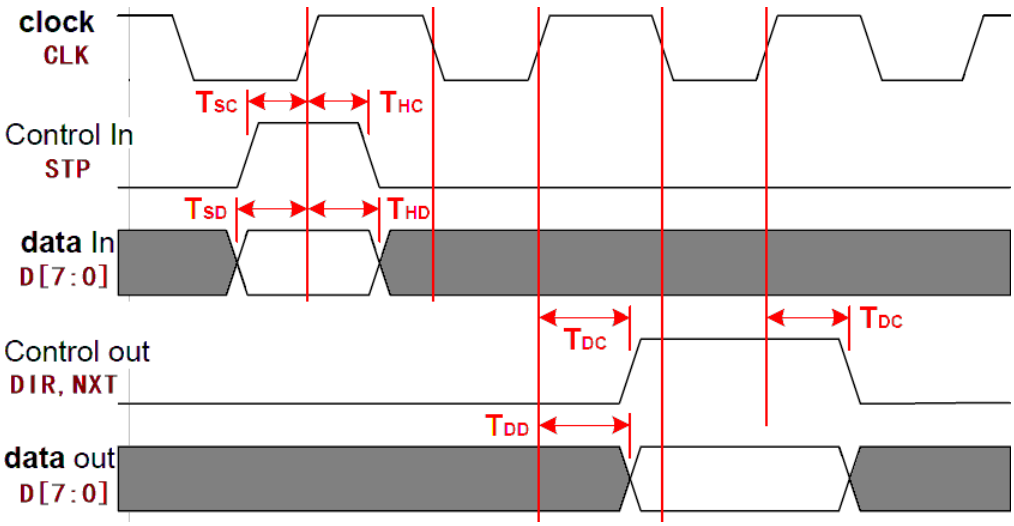
4.2 Electrical characteristics (Test conditions: TA=25°C, V5=5V or V5=VDD33=3.3V, no USB signal pins included)

Symbol	Parameter description		Min.	Typ.	Max.	Unit
V5	LDO input power voltage@V5	LDO enabled	4.5	5.0	5.25	V
	For those with a number in the 4th digit from last of the batch number	LDO enabled	3.7	4.2	4.5	
	External input power voltage@V5	LDO bypassed	3.15	3.3	3.45	
VDD33	LDO output voltage @VDD33	LDO enabled	3.15	3.3	3.45	V
	3.3V external input power source@VDD33	LDO bypassed	3.15	3.3	3.45	
ILDO	Internal power regulator LDO external load capability				30	mA
ICC	Operating current during high-speed USB transfer			27		mA
ICC0	Operating current in the idle state			19		mA
ISLP	Power current in low-power mode			0.1	0.4	mA
VIL	Low level input voltage		0		0.8	V
VIH	High level input voltage		1.9		VDD33	V
VOL	Low level output voltage @ 8mA current input			0.4	0.6	V
VOH	High level output voltage @ 8mA current output		VDD33-0.6	VDD33-0.4		V
IPU	Pull-up current on the STP pin		20	40	80	uA
RPD	Pull-down resistors for pins Date [7:0]		50	70	90	KΩ

Vlvr	Low voltage reset threshold	2.5	2.9	3.15	V

4.3 Timing parameters (Test conditions: TA=25°C, V5=VDD33=3.3V)

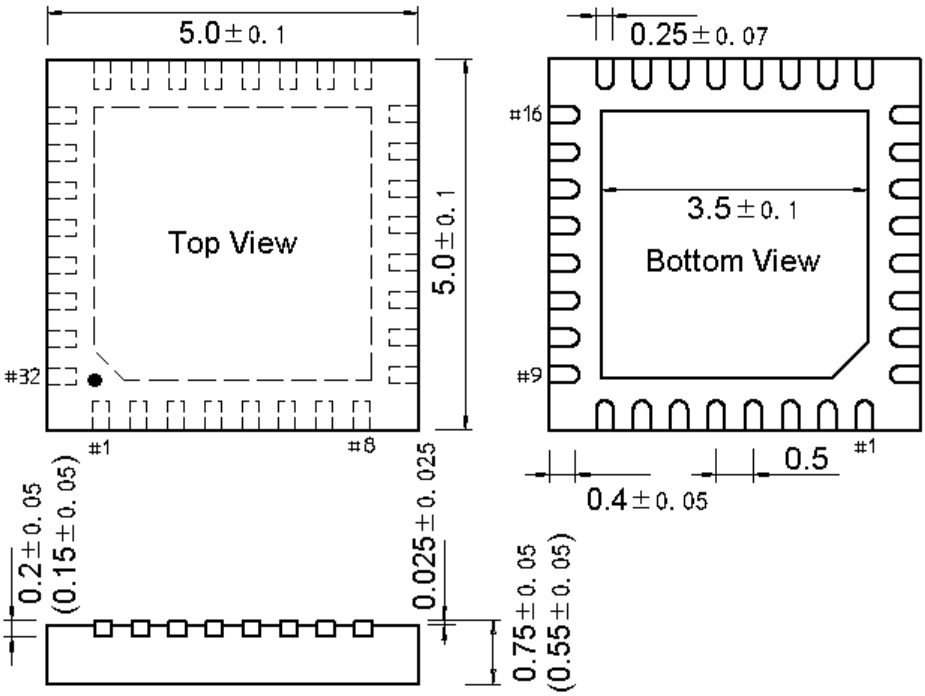
Symbol	Parameter description	Min.	Typ.	Max.	Unit
Fxi	XI input clock frequency, XI external crystal frequency	11.995	12	12.005	MHz
Dutyxi	Duty cycle of XI input clock	35	50	65	%
Fstart	CLK clock frequency of ULPI in the initial state	55	60	65	MHz
Fsteady	CLK clock frequency of ULPI in the steady state	59.97	60	60.03	MHz
Dutycko	Duty cycle of ULPI CLK clock	45	50	55	%
Tsteady	Time from XI input clock stabilization to PLL stabilization		0.5	1.5	mS
Tstart	Time from exit low-power mode to PLL stabilization		2	4	mS
Trpor	Time from power on or low voltage reset to normal operation	10	14	17	mS
Twreset	RESET# pin input reset low level pulse width	2			uS
Trreset	Time from RESET# pin input reset to normal operation	10	13	15	mS
TSC	STP input setup time			6	nS
THC	STP input hold time	2			nS
TSD	Data D0～D7 input setup time			6	nS
THD	Data D0～D7 input hold time	2			nS
TDC	Valid delay time for DIR or NXT output	0.5		6	nS
TDD	Valid delay time for Data D0～D7 output	0.5		9	nS



Chapter 5 Package information

Note:
All dimensions are in millimeters.
The pin center spacing values are nominal, without error. And the error of dimensions other than the pin center spacing values is not more than ±0.2mm.

5.1 QFN32_5x5

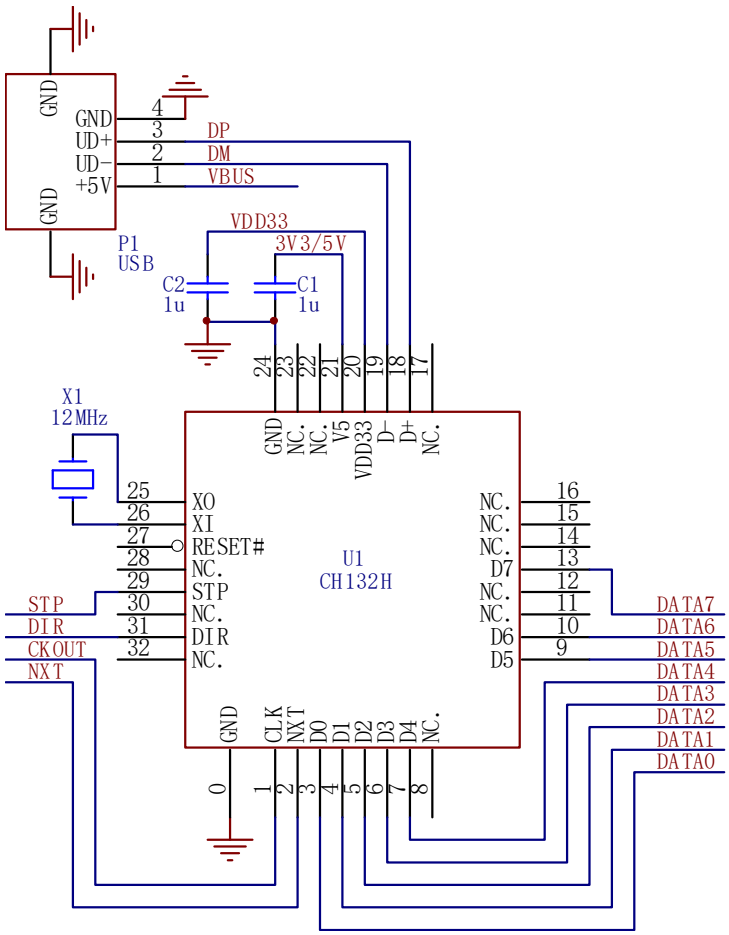


Chapter 6 Applications

6.1 Minimum system

The CH132 acts as a USB PHY for the microcontroller and requires 12 signal lines to be connected. The crystal in the diagram can be replaced by the 12MHz clock provided by the microcontroller or FPGA. The RESET# pin is an optional connection and is left dangling by default. The C1 and C2 capacitors (MLCC) are optional in the 1uF~4.7uF range.

It is recommended that CH132 and the MCU or FPGA use the same 3.3V supply, which is fed from both V5 and VDD33 pins.



6.2 HOST application with VBUS power control

The CH132 is used as a USB PHY for MCU or FPGA, 12 signal lines need to be connected, RESET# pin is an optional connection, the default is left open, if connected, it is recommended that the other driver is set to open-drain output. The MLCC capacitor C2 can be selected in the range of 1uF to 4.7uF.

Both VDD33 and V5 in the diagram use the same external 3.3V supply as the MCU or FPGA.

For USB host applications that also require 5V power to VBUS, it is recommended to consider VBUS overcurrent protection, refer to the diagram below for optional CH217 or similar USB current-limiting power switch chip and control by MCU or FPGA to implement VBUS overcurrent protection. If the internal LDO of CH132 is enabled, it is recommended to replace C2 with two capacitors of 0.1uF and 10uF in parallel to avoid the 5V reduction affecting VDD33 and thus causing CH132 reset. In the figure, the internal LDO is not enabled in CH132.

Simple USB host application can also use 300mA~1A fuse resistor R1 instead of U5, R11, R21 in the figure.

For USB device applications, you can get 5V power from VBUS, refer to the following diagram to remove U5, R11, R21 and C11, and change R1 to 0 or insurance resistor, C4 is reduced to within 10uF according to USB specification. The three power supply schemes are as follows: ①Self-powered 3.3V scheme, without VBUS power, if you need to detect can also be VBUS through the 10KΩ resistor into the MCU pins for detection; ②External LDO step-down scheme, through the external LDO VBUS down to 3.3V for MCU and CH132 use, refer to the following figure U4 step-down; ③Internal LDO step-down scheme, if the MCU power consumption is small, then it can also be unified by the CH132 internal LDO step-down power supply 3.3V, but C2 needs to be increased appropriately, and VBUS needs to add overvoltage protection devices.